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EXAMINER

TRAN, T

ART UNIT

PAPER NUMBER

2811

DATE MAILED: 12/28/99

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.
09/392,865

Applicant(s)
Kitamura et al.

Examiner
Thien Tran

Group Art Unit
2811



☐ Responsive to communication(s) filed on _____

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 35 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) 1-7 is/are pending in the application

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-7 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been received.

☐ received in Application No. (Series Code/Serial Number) _____

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 5

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

— SEE OFFICE ACTION ON THE FOLLOWING PAGES —

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DETAILED ACTION

Election/Restriction

1. Applicant's election without traverse of claims 1-7 in Paper No. 6 is acknowledged.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Japan on 09/09/1998. It is noted, however, that applicant has not filed a certified copy of the prior foreign application as required by 35 U.S.C. 119(b).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim (US 5,834,807) in view of Noda et al. (US 5,068,697) and Santin et al. (US 5,907,171).

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Kim discloses a nonvolatile semiconductor memory device (Fig. 6) comprising a semiconductor substrate; memory transistors formed on said semiconductor substrate to perform nonvolatile storage of an electric charge in accordance with data; protective side walls 62 formed on side walls of gates (46, 50) of each said memory transistor; and a wiring layer 80 formed on an interlayer insulating film 78 of PBSG. Kim does not disclose a second silicon nitride film covering surfaces of said gates, surface of a source diffusion layer (64, 60), surface of a drain diffusion layer (58, 56) and surfaces of said protective side walls 62 of each said memory transistor. Noda et al. discloses a nonvolatile semiconductor memory device (Fig. 4) comprising a silicon nitride film 29 covering the floating gate and control gate, surface of a source diffusion layer 27, surface of a drain diffusion layer 28 and surfaces of protective side walls 26 of each memory transistor. It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate a silicon nitride film into Kim's device covering surfaces of the gates, surface of the source diffusion layer, surface of the drain diffusion layer and surfaces of protective side walls 62 of each said memory transistor in order to prevent a diffusion of metal atoms and transmit oxygen. Kim does not disclose protective side walls 62 being formed of silicon nitride. Silicon oxide and silicon nitride are dielectric materials known in the art and routinely used to form protective side wall spacers in semiconductor device. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select either one of these materials as a suitable dielectric material for protective side walls of Kim, since it has been held to be within the

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general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of design choice. In re Leshin, 125 USPQ 416.

Regarding claim 2, each memory transistor is an electrically rewritable memory transistor including a floating gate 46 over a first gate insulating film 44, and a control gate 50 formed above the floating gate via a second insulating film 48.

Regarding claim 5, the modified Kim does not explicitly disclose metal silicide films formed on surface of the gate and on surfaces of source/drain diffusion layers. It is conventional to form metal silicide films on gate surface and on surfaces of source/drain regions to reduce contact resistance. Therefore, the incorporation of the conventional features into the modified Kim would have been prima facie obvious.

Regarding claim 6, it is evident that the modified Kim discloses the drain diffusion layer (58, 56) connected to a bit line 80 via the metal silicide film and the source diffusion layer (64, 60) connected to a common source line 71 via the metal silicide film respectively.

Regarding claim 7, the modified Kim does not explicitly disclose at least one of a low-voltage MOS transistor and a high-voltage MOS transistor formed as a peripheral circuit. It is conventional to form low-voltage transistor and high-voltage transistor as a peripheral circuit of a memory array, as shown for example by Santin et al. Therefore, the incorporation of the conventional features into the modified Kim would have been prima facie obvious.

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The claim limitations “formed by low-pressure CVD” in claim 1, “deposited by plasma CVD” in claim 3, and “deposited by low-pressure CVD” in claim 4 are taken to be product by process limitations and are given no patentable weight. A product by process claim directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See *In re Fessman*, 180 USPQ 324, 326 (CCPA 1974); *In re Marosi et al.*, 218 USPQ 289, 292 (Fed. Cir. 1983); and particularly *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product “gleaned” from the process steps, which must be determined in a “product by process” claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old and obvious product produced by a new method is not a patentable product, whether claimed in “product by process” claims or not.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Reference D is being cited since it shows a nitride spacer formed on the side wall of a memory cell.

6. **Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group**

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2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Thien Tran* whose telephone number is (703) 308-4108. The Examiner is in the Office generally between the hours of 7:00AM to 5:30PM (Eastern Standard Time) Monday through Thursday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is 308-0956.

Tom Thomas

Tom Thomas
Supervisory Patent Examiner
Technology Center 2800

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December 16, 1999